Claims

What is claimed is:

1. A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

2. The device of claim 1, wherein the shielding structure is connected to the first source/drain region by a conductive trace, the conductive trace being spaced substantially from the gate by an insulating layer formed between the gate and the conductive trace.

3. The device of claim 2, wherein the conductive trace is formed using a metalization process.

4. The device of claim 2, wherein the conductive trace is formed using at least a second level metalization process.

5. The device of claim 2, wherein the insulating layer comprises an oxide.

6. The device of claim 1, wherein the first source/drain region is a source of the device and the second source/drain region is a drain of the device.

7. The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

8. The device of claim 1, wherein the device comprises a laterally diffused MOS (LDMOS) device.

9. The device of claim 1, wherein the device comprises a vertical diffused MOS device.

10. The device of claim 1, wherein the shielding structure is formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region.

11. The device of claim 1, wherein the shielding structure comprises at least one conductive plug.

12. The device of claim 1, further comprising a conductive layer formed on an upper surface of the gate such that the conductive layer substantially covers the upper surface of the gate, whereby a resistance of the gate is reduced.

13. The device of claim 1, further comprising an insulting layer formed on at least a portion of an upper surface of the device, the shielding structure comprising a conductive plug formed at least partially through the insulating layer.

14. An integrated circuit including at least one metal-oxide-semiconductor (MOS) device, the at least one MOS device comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

15. The integrated circuit of claim 14, wherein the shielding structure in the at least one MOS device is connected to the first source/drain region by a conductive trace, the conductive trace being spaced substantially from the gate by an insulating layer formed between the gate and the conductive trace.

16. The integrated circuit of claim 14, wherein the at least one MOS device comprises a laterally diffused MOS (LDMOS) device.

17. The integrated circuit of claim 14, wherein the shielding structure in the at least one MOS device is formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region.

18. The integrated circuit of claim 14, wherein the at least one MOS device further comprises a conductive layer formed on an upper surface of the gate such that the conductive layer substantially covers the upper surface of the gate, whereby a resistance of the gate is reduced.